

FIG 1

using any other means, such as, for example, a computer, to determine the value of the function $f(x)$ at the point x and to compare the value of the function $f(x)$ at the point x with the value of the function $f(x)$ at the point x_0 .

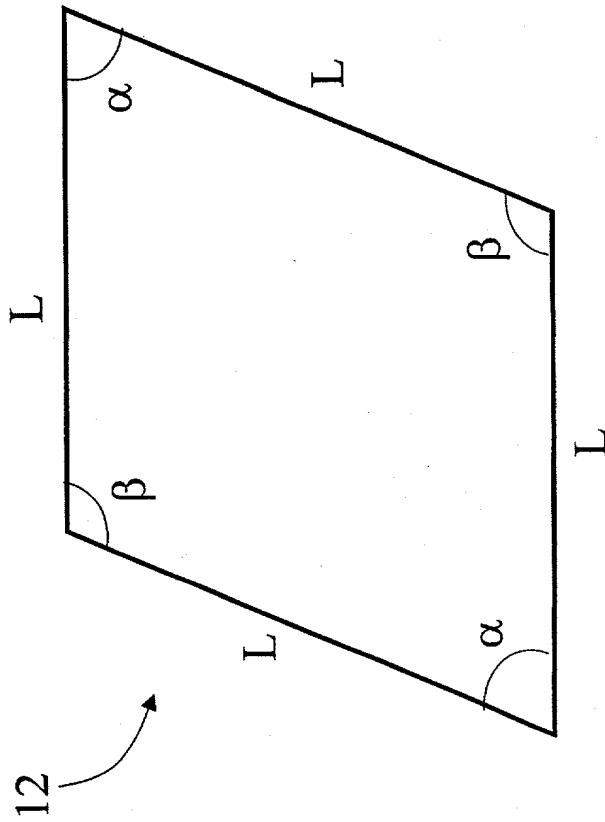


FIG 2

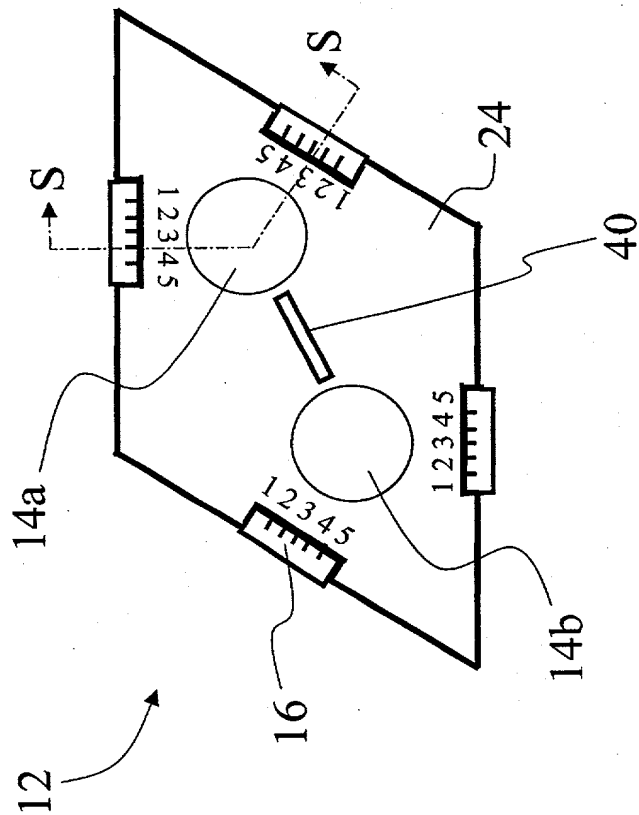


FIG 3

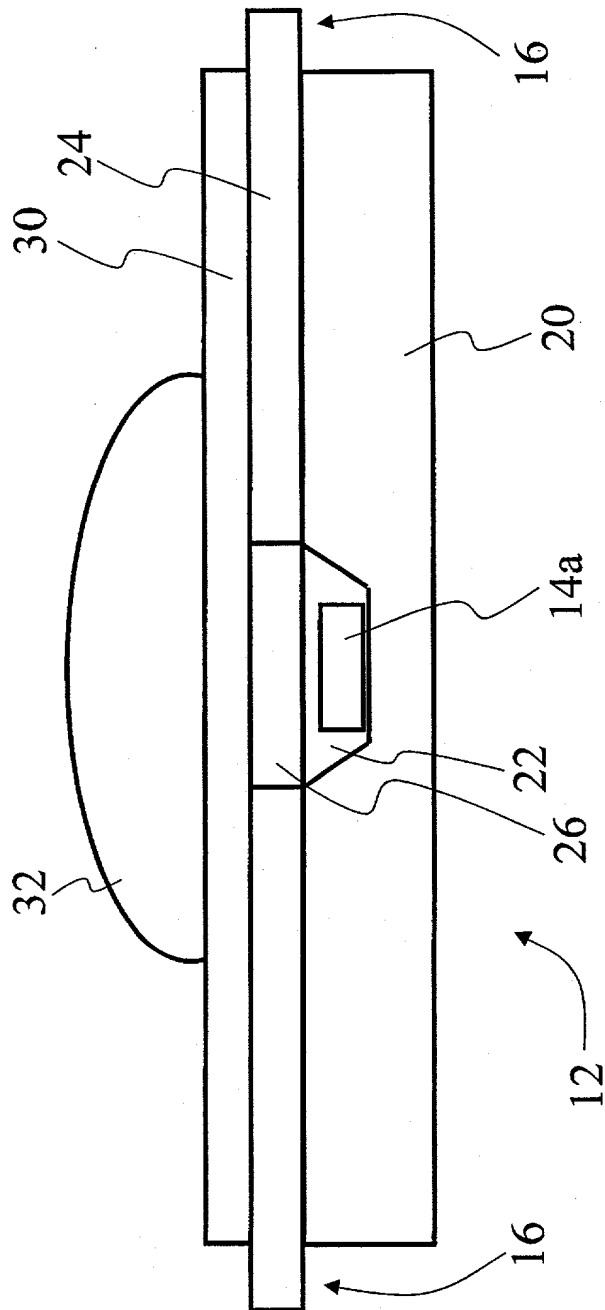


FIG 4

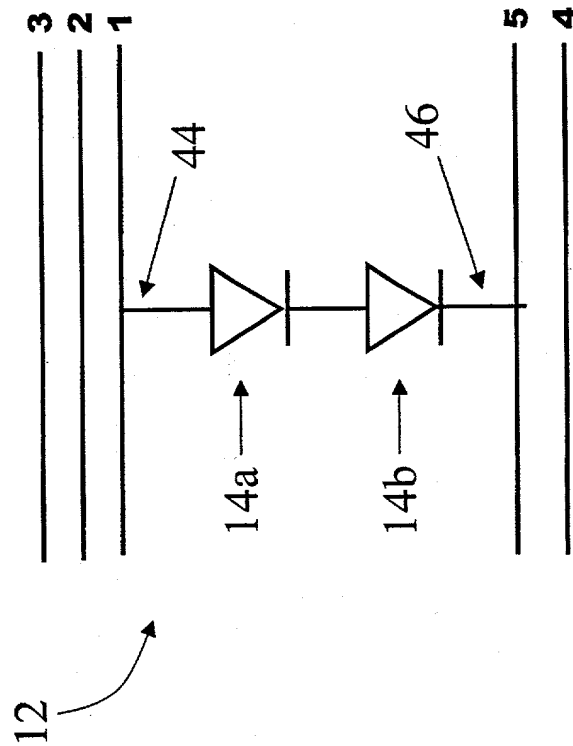


FIG 5

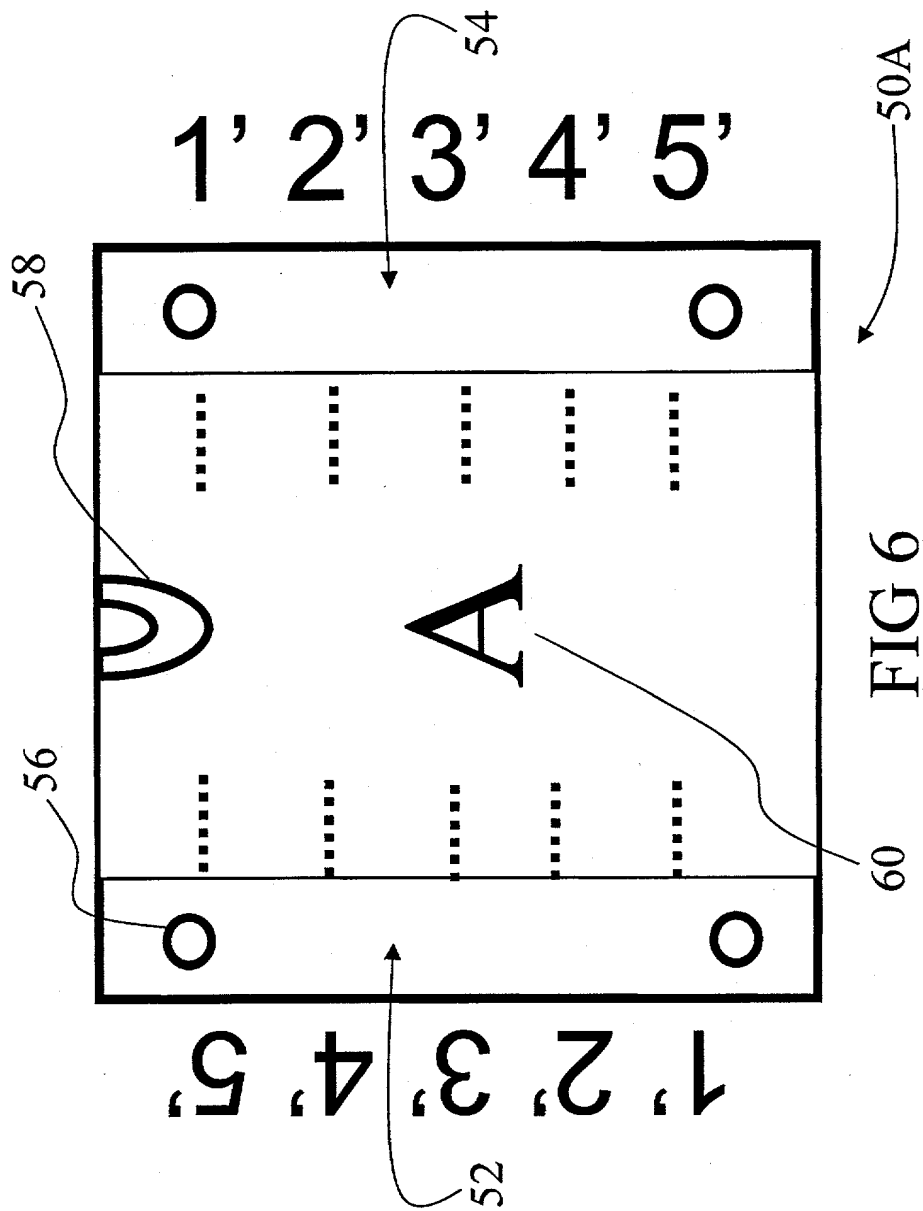


FIG 6

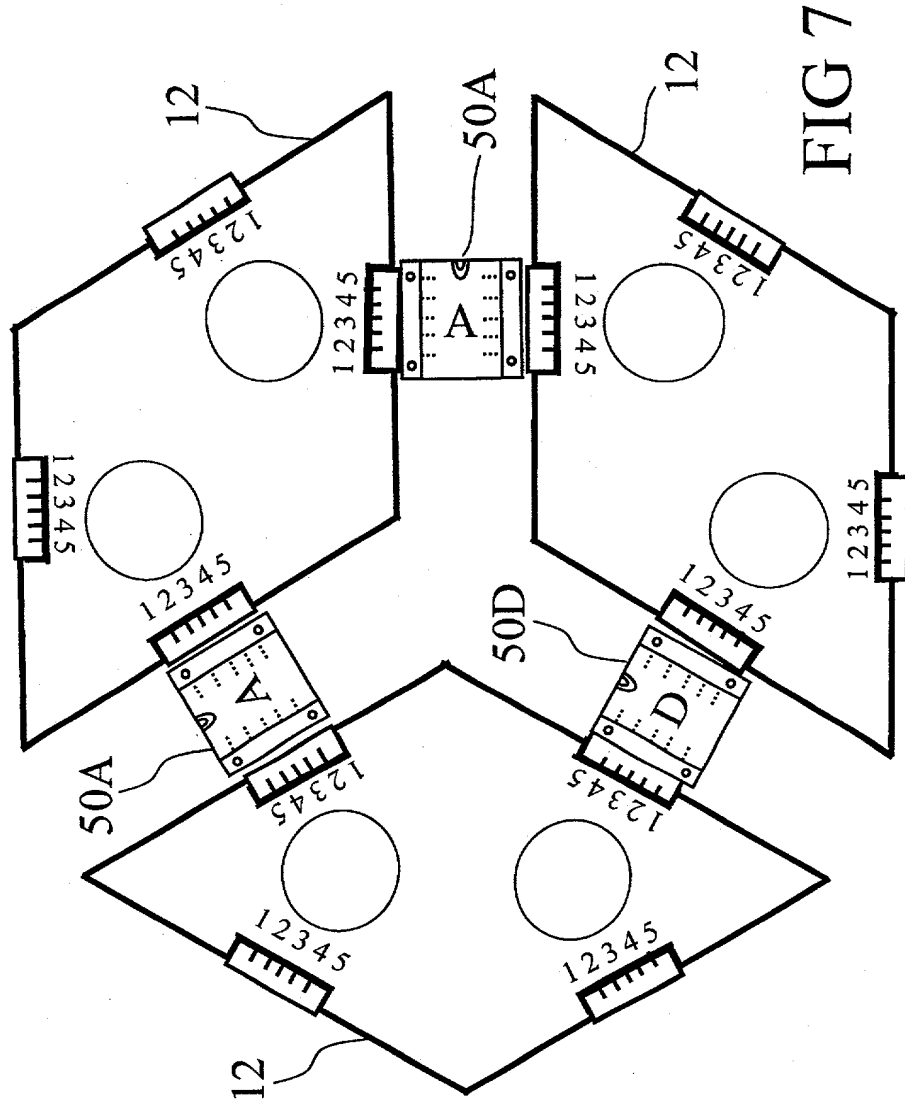


FIG 7

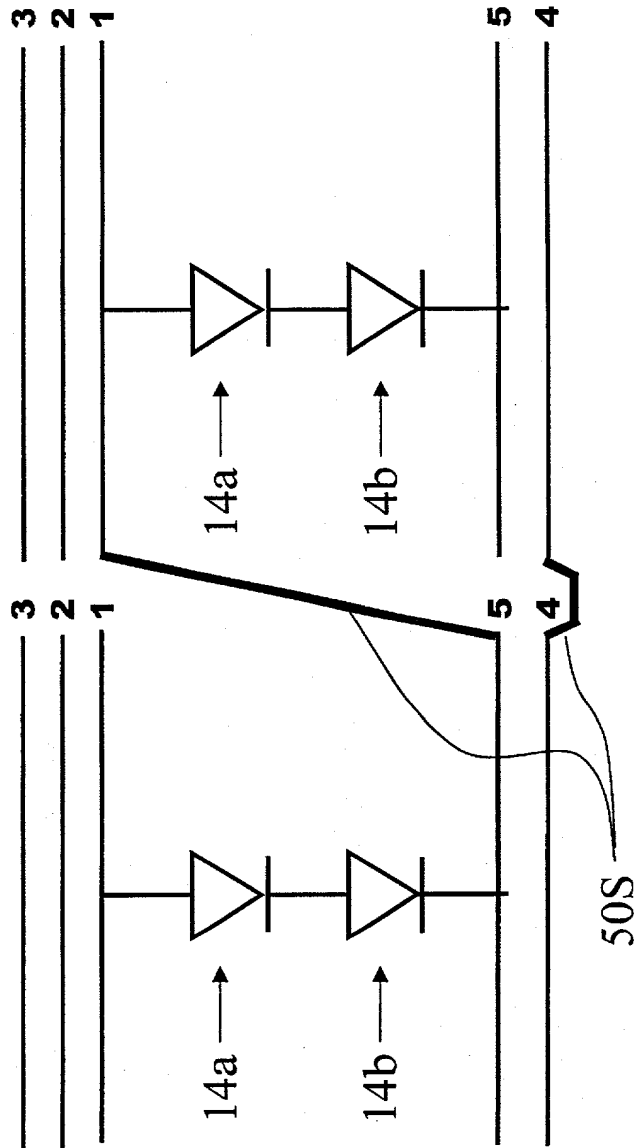
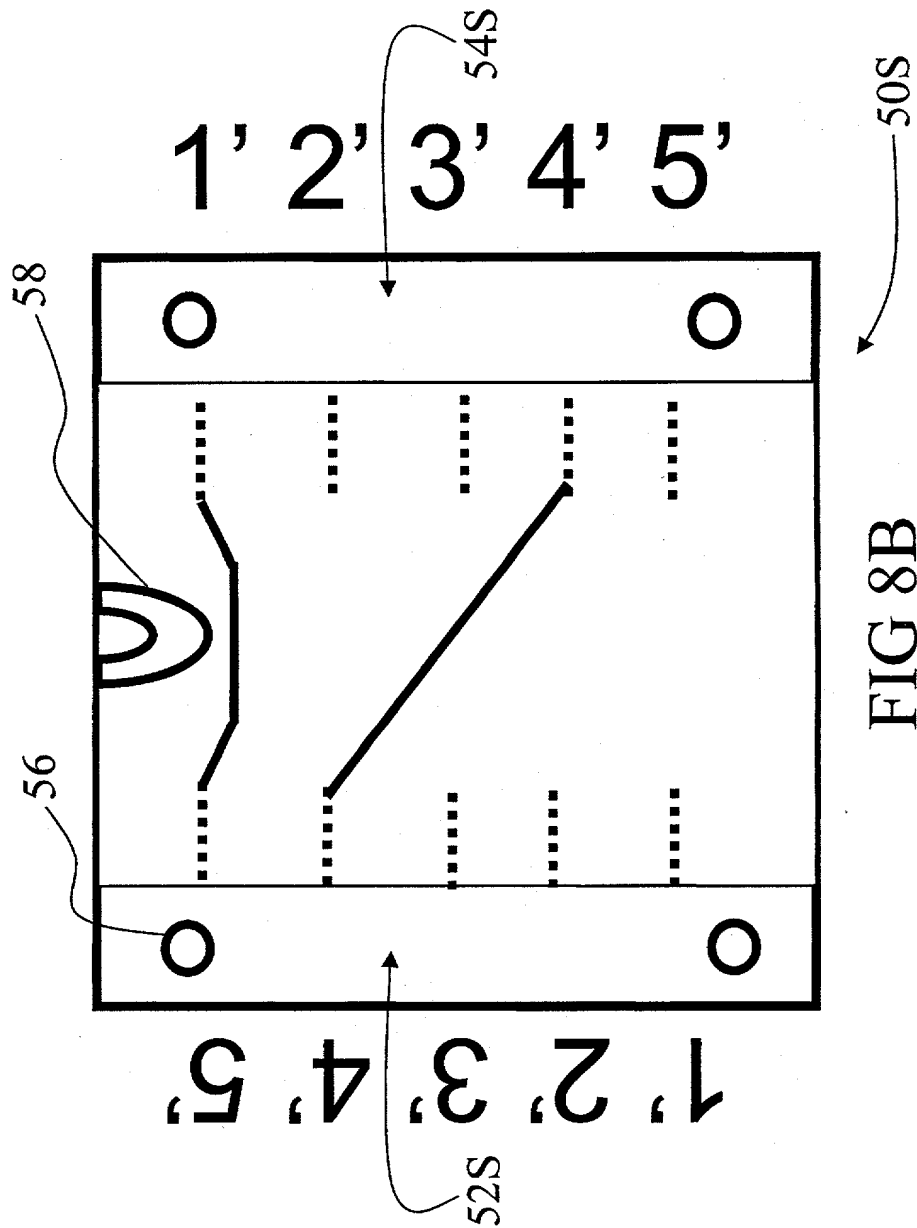


FIG 8A



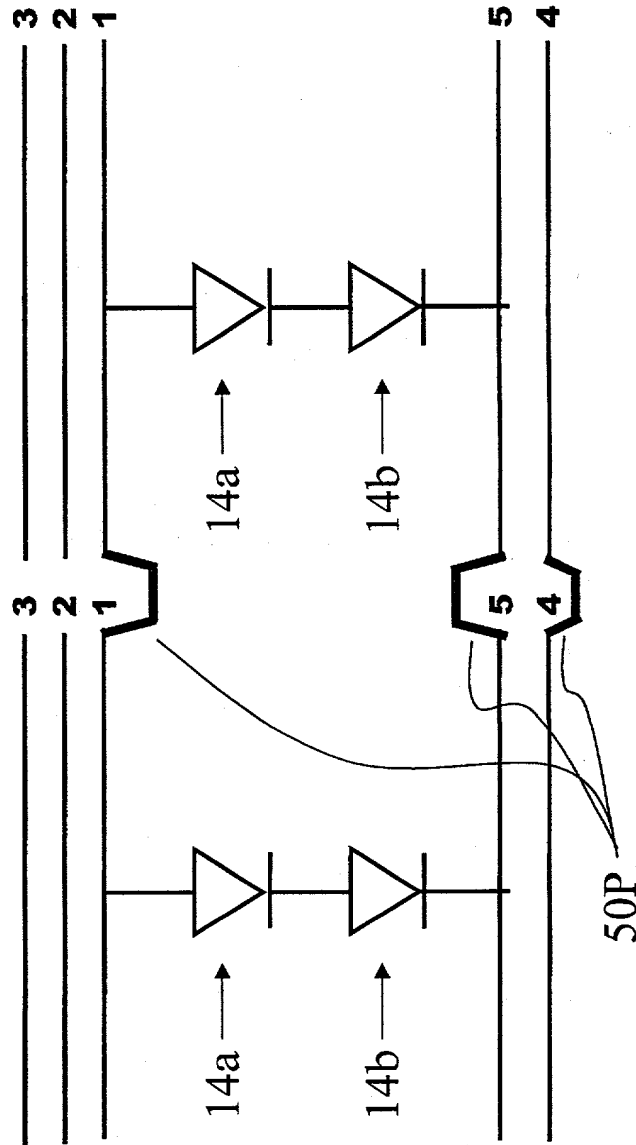


FIG 9A

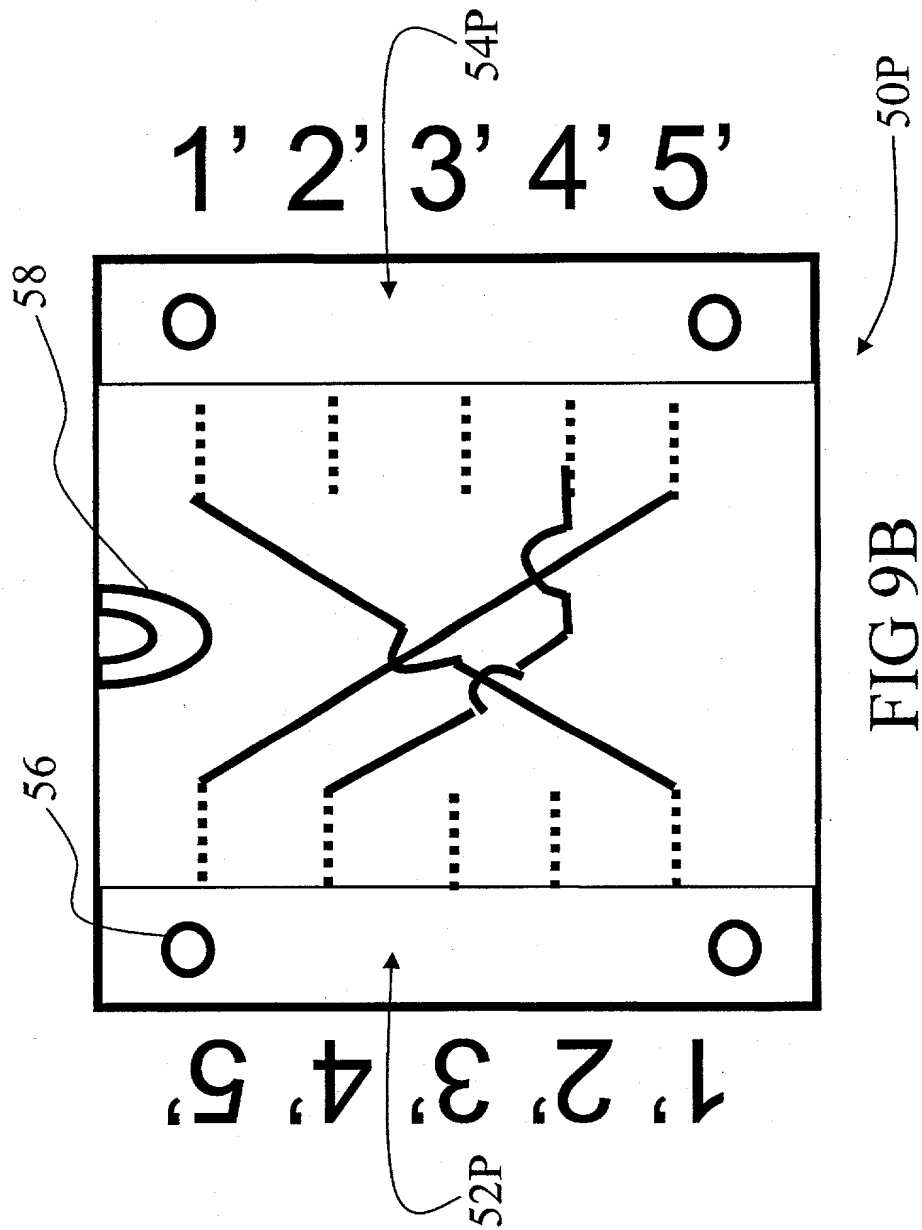


FIG 9B

FIG. 10A is a schematic diagram of a semiconductor device. The device includes a substrate 100 with a first conductive layer 102, a second conductive layer 104, and a third conductive layer 106. A first gate stack 110 is formed on the substrate 100, and a second gate stack 112 is formed on the substrate 100. A first channel region 120 is formed in the substrate 100, and a second channel region 122 is formed in the substrate 100. A first source region 130 is formed in the substrate 100, and a second source region 132 is formed in the substrate 100. A first drain region 140 is formed in the substrate 100, and a second drain region 142 is formed in the substrate 100. A first gate electrode 144a is formed on the first gate stack 110, and a second gate electrode 144b is formed on the second gate stack 112. A first gate electrode 144a is formed on the first gate stack 110, and a second gate electrode 144b is formed on the second gate stack 112. A first gate electrode 144a is formed on the first gate stack 110, and a second gate electrode 144b is formed on the second gate stack 112.

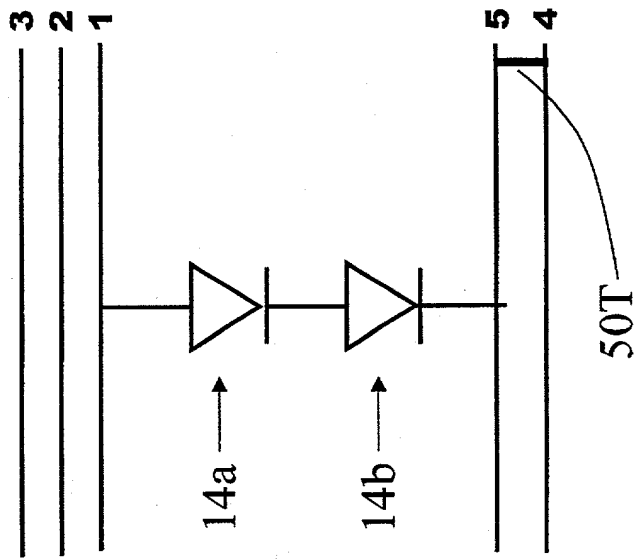


FIG 10A

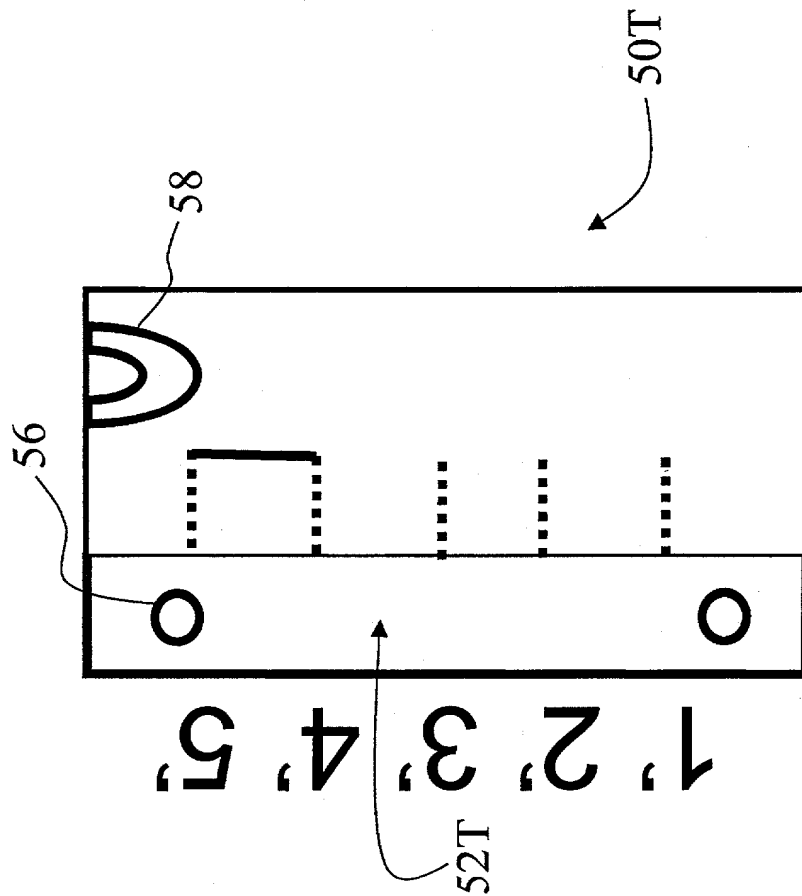


FIG 10B

FIG. 11B is a schematic diagram of a device 50. The device 50 includes a rectangular frame 54 and a central region 56. The central region 56 is divided into five vertical sections labeled 1', 2', 3', 4', and 5'. Each section contains a vertical dashed line. The device 50 is connected to a power source 64 via a cable 62. The power source 64 is a battery with a positive terminal (+) and a negative terminal (-). The device 50 also includes a component 58 on the left side.

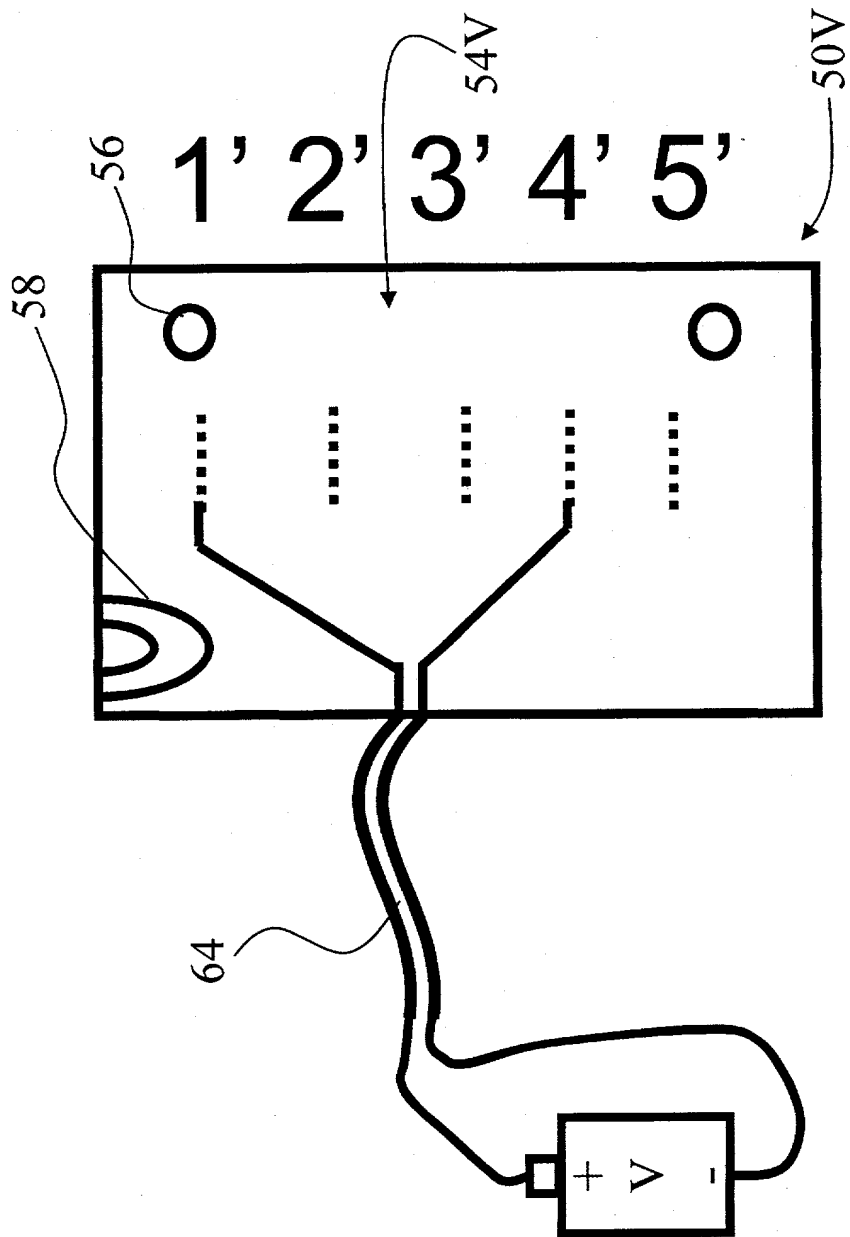
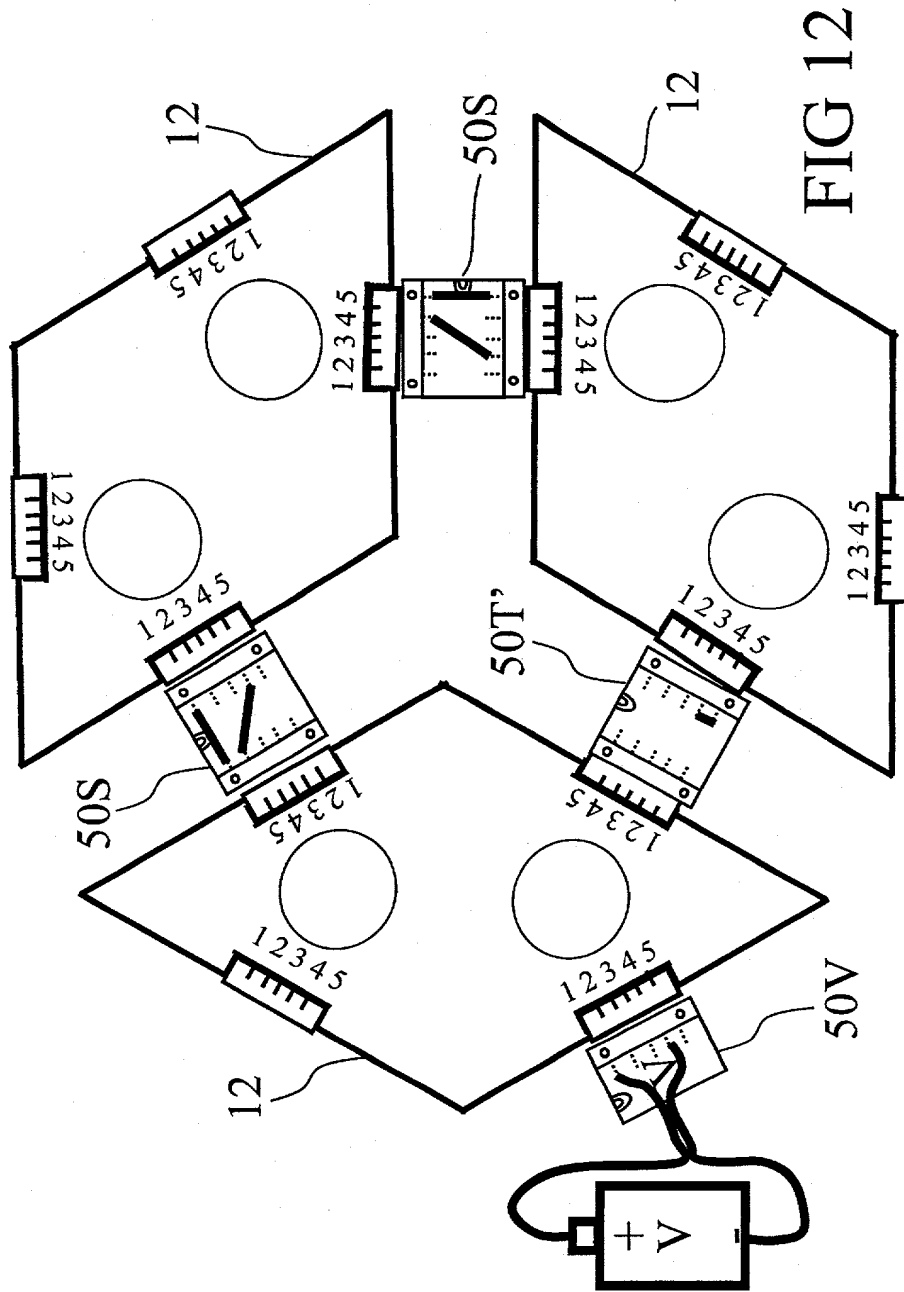


FIG 11B

FIG. 12 is a schematic diagram of a circuit for testing a device under test (DUT) 12. The circuit includes a power source 50V, a switch 50S, and a load 50T. The DUT 12 is connected to the power source 50V through the switch 50S and the load 50T. The circuit is configured to measure the current flowing through the DUT 12 and the power dissipated by the load 50T.



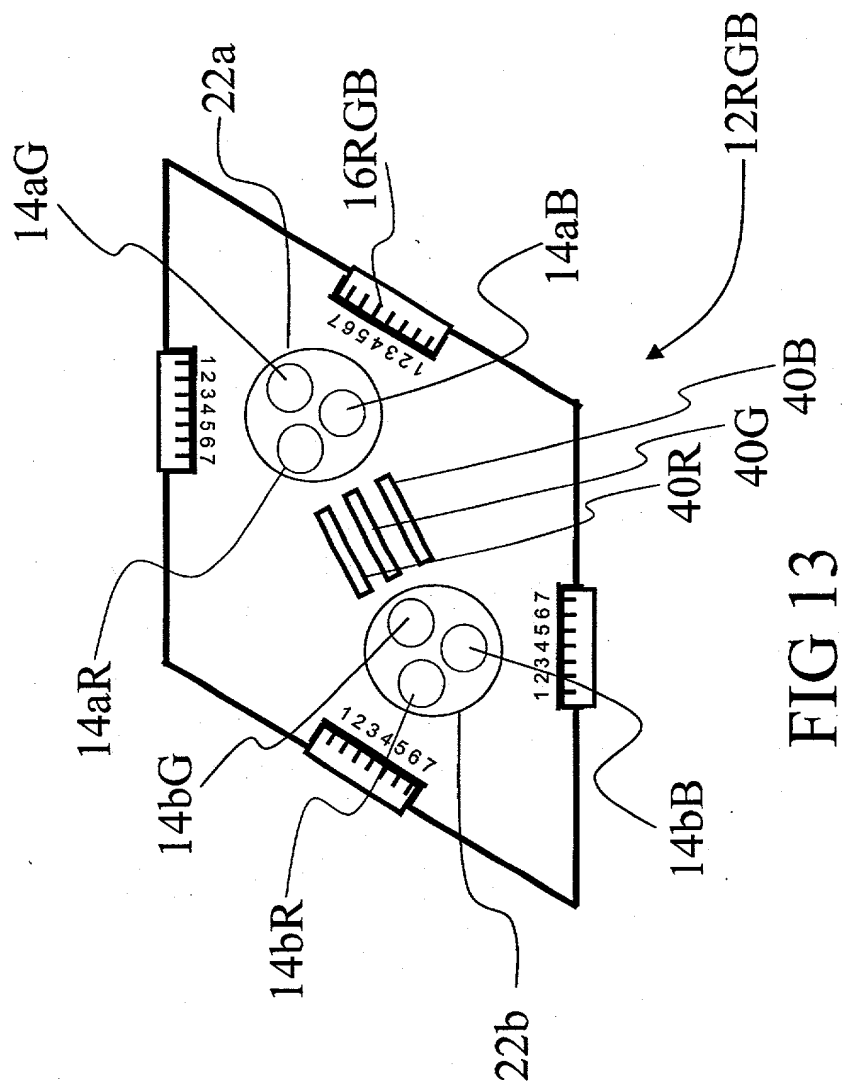


FIG 13

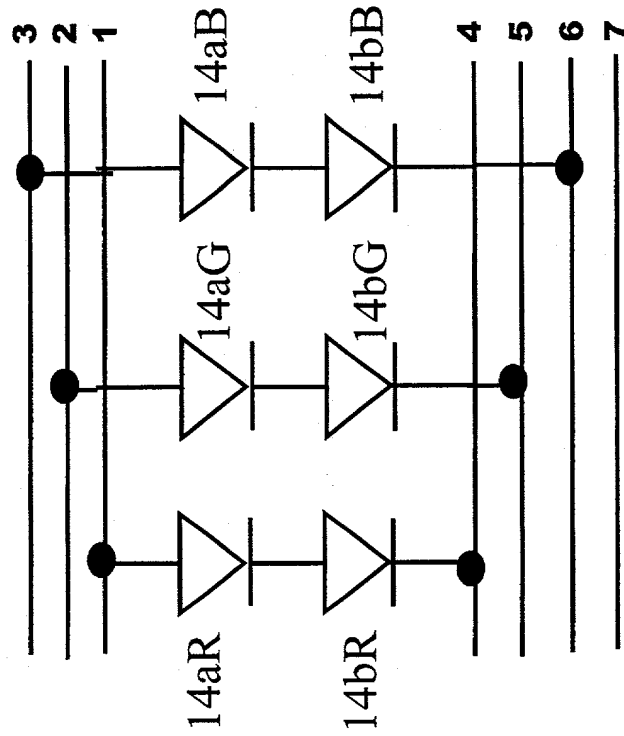


FIG 14

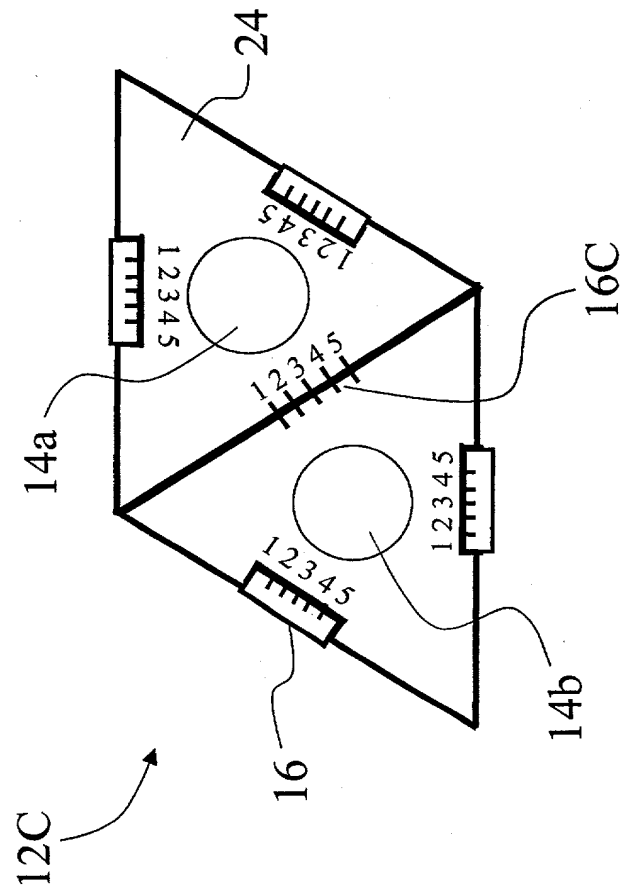


FIG 15

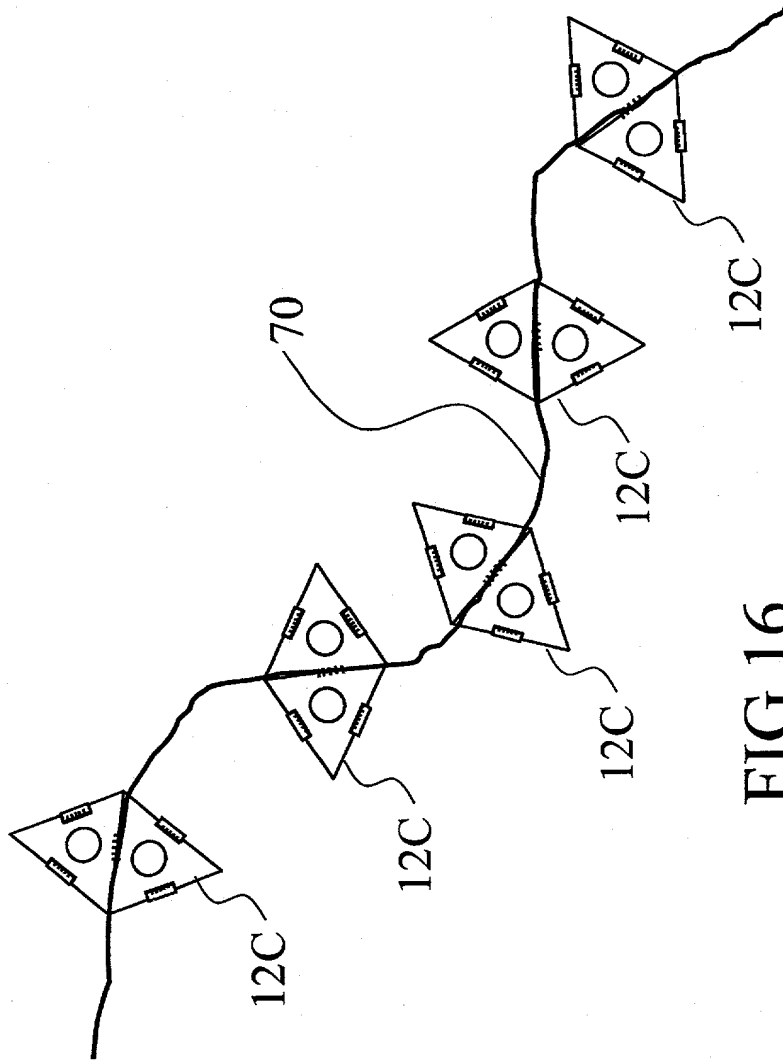


FIG 16